CLAIMS

We claim:

1. A trapped charge memory device comprising:

a top electrode;

a bottom electrode; and

a trapped charge memory body sandwiched between and in electrical contact with said top electrode and said bottom electrode, defining both a top electrode to trapped charge memory body contact and a bottom electrode to trapped charge memory body contact;

wherein said trapped charge memory device contains current carrier traps that influence said trapped charge memory device's voltage switchable resistance R_d;

whereby said influence of R_d is accomplished with energy levels of said current carrier traps, degrees of carrier occupancy or concentration of said current carrier traps, or some combination thereof.

2. The trapped charge memory device of claim 1 wherein said current carrier traps comprise electron traps.

3. The trapped charge memory device of claim 1 wherein said current carrier traps comprises hole traps.

4. The trapped charge memory device of claim 1 wherein said current carrier traps are characterized by at least one energy level within a bandgap between a conduction band and a valence band of said trapped charge memory body for trapping current carriers.

5. The trapped charge memory device of claim 1 wherein the energy levels and respective degrees of carrier occupancy of said current carrier traps are selected such that said trapped charge memory device, while under a variable drive voltage of V_d applied

between said top electrode and said bottom electrode, exhibiting M voltage switchable levels of resistance values $R_1, R_2, \ldots, R_M$ in the following manner:

$R_d = R_j$ when $-VN_{cj} <= V_d <= +VP_{cj}$; and

R_d switches to R_{j+1} when V_d goes above $+VP_{cj}$ followed by R_d switching back to R_j when V_d then drops below $-VN_{cj}$

where $M >= 2$, $j = (1, 2, \ldots, M-1)$ and each of VP_{cj} and VN_{cj} are positive voltage magnitudes.

6. The trapped charge memory device of claim 5 wherein VP_{cj} is essentially equal to VN_{cj} for at least one value of the index j whereby the corresponding switching of R_d between R_j and R_{j+1} uses a symmetric bipolar drive operation in the voltage domain.

7. The trapped charge memory device of claim 5 wherein the resistance switching time, between members of the resistance values $R_1, R_2, \ldots$ and R_M, of said R_d is from about 0.1 ns to about 100 μs.

8. The trapped charge memory device of claim 1 wherein at least one of the top electrode-to-trapped charge memory body contact and the bottom electrode-to-trapped charge memory body contact is made non-ohmic, whereby said R_d exhibits a corresponding degree of nonlinearity.

9. The trapped charge memory device of claim 1 wherein said R_d is a function of the total charge, called trapped charges, carried by trapped current carriers at said current carrier traps.

10. The trapped charge memory device of claim 9 wherein the amount of trapped charges is modifiable by the height and width of a write voltage pulse applied across said top electrode and said bottom electrode.

11. The trapped charge memory device of claim 9 wherein the amount of trapped charges is modifiable by a mechanism of carrier tunneling.

12. The trapped charge memory device of claim 9 wherein the amount of trapped charges is modifiable by a mechanism of free carrier capturing.

13. The trapped charge memory device of claim 1 wherein said R_d is a function of trapped charges located within the bulk of the trapped charge memory body.

14. The trapped charge memory device of claim 1 wherein said R_d is a function of current carrier traps located within two Schottky junctions respectively defined by said top electrode-to-trapped charge memory body contact and said bottom electrode-to-trapped charge memory body contact.

15. The trapped charge memory device of claim 14 wherein said current carrier traps acts, depending upon their charge type, to alter the barrier height of said Schottky junctions thus effecting a corresponding change of R_d.

16. The trapped charge memory device of claim 1 wherein said R_d is a function of current carrier traps located near any of said top electrode-to-trapped charge memory body contact or said bottom electrode-to-trapped charge memory body contact that is a Schottky junction.

17. The trapped charge memory device of claim 16 wherein said current carrier traps acts, depending upon their charge type, to alter the barrier height of said Schottky junction thus effecting a corresponding change of R_d.

18. The trapped charge memory device of claim 1 wherein most of said current carrier traps are located near said top electrode.

19. The trapped charge memory device of claim 1 wherein most of said current carrier traps are located near said bottom electrode.

20. The trapped charge memory device of claim 1 wherein most of said current carrier traps are located near either said top electrode or said bottom electrode.

21. The trapped charge memory device of claim 1 wherein said current carrier traps are distributed throughout the bulk of said trapped charge memory body.

22. The trapped charge memory device of claim 1 wherein said current carrier traps are located at the interface between at least one electrode and said trapped charge memory body.

23. The trapped charge memory device of claim 1 wherein said R_d is a function of those current carrier traps capable of altering the conductivity of the trapped charge memory body.

24. The trapped charge memory device of claim 23 wherein said current carrier traps are, through an electrical force interaction with nearby current carriers, capable of reducing the conductivity of the trapped charge memory body.

25. The trapped charge memory device of claim 23 wherein said current carrier traps are, through an electrical force interaction with nearby current carriers, capable of increasing the conductivity of the trapped charge memory body.

26. The trapped charge memory device of claim 1 wherein said R_d is a function of those current carrier traps capable of effecting a trap-hopping type of conduction mechanism.

27. The trapped charge memory device of claim 1 wherein said R_d is a function of those current carrier traps capable of effecting a Frenkel-Poole type of conduction mechanism.

28. The trapped charge memory device of claim 1 wherein said R_d is a function of those current carrier traps capable of disrupting the preferred direction of an ordered pattern of the electron orbitals within a crystal lattice of said trapped charge memory body.

29. The trapped charge memory device of claim 1 wherein said R_d is a function of those current carrier traps capable of affecting an electron tunneling mechanism.

30. The trapped charge memory device of claim 1 wherein said current carrier traps are created within said trapped charge memory body with the addition of a dopant.

31. The trapped charge memory device of claim 30 wherein said trapped charge memory body is made of a crystalline structure and said dopant material is substitutionally fit into said crystalline structure.

32. The trapped charge memory device of claim 30 wherein said trapped charge memory body is made of a crystalline structure and said dopant material is interstitially fit into said crystalline structure.

33. The trapped charge memory device of claim 30 wherein said dopant material is implemented as separate physical clusters within said trapped charge memory body material.

34. The trapped charge memory device of claim 1 wherein

said trapped charge memory body includes a p-type region that interfaces with an n-type region, such that a space charge region is formed; and

said current carrier traps are located primarily in the space charge region of the trapped charge memory body.

35. The trapped charge memory device of claim 1 wherein said trapped charge memory body is made of an insulator, a conductor, a conductive oxide, a polymer, organic molecules, carbon nanotubes or a semiconductor.

36. The trapped charge memory device of claim 1 wherein said trapped charge memory body comprises a poly-crystalline material and said current carrier traps are created at the grain boundaries of said poly-crystalline material.

37. The trapped charge memory device of claim 1 wherein said trapped charge memory body is a layer of thickness between about 100Å and about 5000Å.

38. A method of making a 2-terminal trapped charge memory device with voltage switchable multi-level resistance R_d and having a top electrode, a bottom electrode and a trapped charge memory body sandwiched between and in electrical contact with said top electrode and said bottom electrode defining a top electrode-to-trapped charge memory body contact and a bottom electrode-to-trapped charge memory body contact, said trapped charge memory body containing current carrier traps with at least one of whose energy levels, respective degrees of carrier occupancy and concentration determine said R_d, the method comprising:

providing a substrate;

forming a bottom electrode layer atop said substrate;

forming a trapped charge memory body layer atop and in electrical contact with said bottom electrode layer; and

forming a top electrode layer atop and in electrical contact with said trapped charge memory body layer.

39. The method of making a 2-terminal trapped charge memory device of claim 38 further comprising creating current carrier traps within said trapped charge memory body through a conditioning procedure.

40. The method of making a 2-terminal trapped charge memory device of claim 39 wherein said conditioning procedure imparts said current carrier traps with a desired degree of carrier occupancy.

41. The method of making a 2-terminal trapped charge memory device of claim 40 wherein said conditioning procedure includes high energy radiation, particle beam bombardment or an electrical initialization process.

42. The method of making a 2-terminal trapped charge memory device of claim 41 wherein said high energy radiation includes exposing the trapped charge memory device with X-ray or UV light.

43. The method of making a 2-terminal trapped charge memory device of claim 41 wherein said electrical initialization process includes exposing the trapped charge memory device with an electrical field.

44. The method of making a 2-terminal trapped charge memory device of claim 38 wherein one or both of the top electrode-to-trapped charge memory body contact and the bottom electrode-to-trapped charge memory body contact are made non-ohmic to create a corresponding nonlinearity of R_d.

45. The method of making a 2-terminal trapped charge memory device of claim 38 wherein said trapped charge memory body layer is made of a semiconducting material of single-crystalline, poly-crystalline or amorphous structure.

46. The method of making a 2-terminal trapped charge memory device of claim 39 wherein the conditioning procedure is performed after the top electrode is formed.

47. The method of making a 2-terminal trapped charge memory device of claim 46 wherein said conditioning procedure imparts said current carrier traps with a desired degree of carrier occupancy.

48. The method of making a 2-terminal trapped charge memory device of claim 47 wherein said conditioning procedure includes high energy radiation, particle beam bombardment or an electrical initialization process.

49. The method of making a 2-terminal trapped charge memory device of claim 48 wherein said high energy radiation includes exposing the trapped charge memory device with X-ray or UV light.

50. The method of making a 2-terminal trapped charge memory device of claim 48 wherein said electrical initialization process further comprises exposing the trapped charge memory device with an electrical field.

51. The method of making a 2-terminal trapped charge memory device of claim 46 wherein one or both of the top electrode-to-trapped charge memory body contact and the bottom electrode-to-trapped charge memory body contact are made non-ohmic to create a corresponding nonlinearity of R_d.

52. The method of making a 2-terminal trapped charge memory device of claim 46 wherein said trapped charge memory body layer is made of a semiconducting material of single-crystalline, poly-crystalline or amorphous structure.

53. The method of making a 2-terminal trapped charge memory device of claim 39 wherein the conditioning procedure is performed after the top electrode is formed and the conditioning procedure imparts said current carrier traps with a desired degree of carrier occupancy.

54. The method of making a 2-terminal trapped charge memory device of claim 53 wherein the charge conditioning procedure includes exposure of the trapped charge memory device to UV light.

55. The method of making a 2-terminal trapped charge memory device of claim 53 wherein the charge conditioning procedure includes exposure of the trapped charge memory device to an electric current.

56. The method of making a 2-terminal trapped charge memory device of claim 53 wherein the charge conditioning procedure includes exposure of the trapped charge memory device to an electric field.